Abstract of the Disclosure

A NAND-type flash memory device including a memory cell array having a plurality of memory blocks is provided. An example NAND-type flash memory device includes a status cell array which has a plurality of status cells and stores data indicating erase/program statuses of the memory blocks, a data generation circuit which generates data indicating a program status of a selected memory block in response to a data input command and generates data indicating an erase status of a selected memory block in response to a block erase setup command, a first signal generation circuit which generates a block status write enable signal and a clock signal in response to either one of an erase command and a program command, a selection circuit which selects at least one of the status cells of the status cell array in response to a block address of the selected memory block, a write circuit which receives data from the data generation circuit in response to the clock signal during a program or erase operation and writes the received data in the selected status cell, and a control circuit which operates in response to a block status write enable signal from the first signal generation circuit and controls the write circuit so as to the store the data inputted to the write circuit in a selected status cell when an erase/program operation for the selected memory block is carried out.